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09/756,793	01/10/2001	Takashi Kaku	21.1990	6546

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EXAMINER	
VARTANIAN, HARRY	

ART UNIT	PAPER NUMBER
2634	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/756,793	Applicant(s) KAKU ET AL.	
	Examiner Harry Vartanian	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 9* is/are allowed.

6)☒ Claim(s) *1,4-6 and 8* is/are rejected.

7)☒ Claim(s) *2 ,3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. Specification is objected to for a minor informality. There is typo on page 14, line 7. Please change "roll of filter" to "roll off filter". Appropriate correction is required.

2. On page 13, line 10 the specification refers to communication lines 32. The drawings show that the communications lines are labeled as item 30. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 4, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Millward et al(US Patent# 6,324,228). Regarding Claim 1, Millward et al meets the following limitations:

An automatic gain control circuit**(abstract; fig 4 item 440)** comprising:

> a first error calculation circuit which calculates an amount of first error between an input signal and a first reference, and outputs a first signal corresponding to said first error; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

a second error calculation circuit which calculates an amount of second error between an input signal and a second reference, and outputs a second signal corresponding to said second error; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

a determination circuit connected to said first error calculation circuit and said second error calculation circuit, determines a value of an output signal from said first error calculation circuit, and selects one of said first and second signals based on said determination; and **fig 6 (Column 6, Line 13 to Column 7, Line 29); Fig 7, item 730;**

Millward et al fails to teach the use of an integrator in his AGC controller.

However, in the applicant's admitted prior art the use an integrator in an AGC circuit is disclosed in fig 5 and page 2. Therefor it would have been prima facie obvious at the time the invention was made for an integrator to be used in an AGC circuit. The motivation to combine is that the integrator sums up the "accumulated errors" between the input signal and threshold value which is then used by the second multiplier to adjust the signal outputted from the equalizer(applicant states this in the last paragraph of page 2).

Regarding Claim 4, Millward et al meets the following limitations:

an automatic gain controller**(abstract; fig 4 item 440)**, connected to said equalizer, to control a level of an input signal to be stabilized in a constant value; **abstract**

wherein, said automatic gain controller comprising: a first error calculation circuit for calculating a first error value between an input signal and a first reference signal; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

a second error calculation circuit for calculating a second error value between an input signal and a second reference signal; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

a determination module, connected to said first error calculation circuit, said second error calculation circuit and said integrating circuit, for determining whether an output signal of said integrating circuit is larger than said predetermined value, and **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

selecting one of said first error calculation circuit and said second error calculation circuit for an automatic gain control based on said determination. **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

Millward et al fails to teach the use of an integrator or equalizer in his AGC controller.

However, the limitation regarding the use of an integrator was meet in the above paragraph. Furthermore, in the applicants admitted prior art the use of an equalizer connected to the AGC circuit is disclosed in figure 5. Therefor it would have been prima facie obvious at the time the invention was made for an AGC circuit to use an equalizer. The

motivation to combine is that an equalizer is needed to reverse the harmful effects a channel has on a signal during transmission.

Regarding Claim 5, Millward et al also fails to Claim that his AGC circuit uses a squaring circuit. However, in the applicant's admitted prior art the use of a squaring circuit in an AGC circuit is disclosed in fig 5 and page 2. Therefor it would have been prima facie obvious at the time the invention was made for a squaring circuit to be used in an AGC circuit. The motivation to combine is that a squaring circuit is needed in order to calculate the power of the input signal, which is then used by the comparator to compare it against some threshold value.

Regarding Claim 6, Millward et al also fails to Claim that his AGC circuit uses a rectifying circuit. However, in the applicant's admitted prior art the use of a rectifying circuit in an AGC circuit is disclosed in fig 5 and page 2. Therefor it would have been prima facie obvious at the time the invention was made for a rectifying circuit to be used in an AGC circuit. The motivation to combine is that a rectifier can be used by AGC to calculate the absolute value of a signal, which is then used to compare the power of received signal to a threshold level. (Please see US Patent #4,689,805 Column 5, Lines 60-65 incorporated by reference)

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Millward et al(US Patent# 6,324,228). Regarding Claim 8, Millward et al meets the following limitations:

> An automatic gain control**(abstract; fig 4 item 440)** method comprising:
>
> calculating a first error between an input signal and a first reference; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

calculating a second error between an input signal and a second reference; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

determining a value of said first error; selecting one of said first error and said second error as an output based on said determination; **fig 6 (Column 6, Line 13 to Column 7, Line 29);**

Millward et al fails to teach integrating the selected output in his AGC controller.

However, in the applicant's admitted prior art the use of integration in an AGC circuit is disclosed in fig 5 and page 2. Therefor it would have been prima facie obvious at the time the invention was made for integrating the output of an AGC circuit. The motivation to combine is that the integrator sums up the "accumulated errors" between the input signal and threshold value which is then used by the second multiplier to adjust the signal outputted from the equalizer(applicant states this in the last paragraph of page 2).

Allowable Subject Matter

4. Claims 7 and 9 are allowed. Regarding Claim 7, the prior art failed to teach the specific operation of the determination module and the use of a second integrator in the AGC circuit(lines 1-8).

Regarding Claim 9, the prior art failed to teach the specific operation of selecting either the first error or second error result in an AGC circuit.

5. Claims 2, 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. It is highly recommended that all the references made in PTO-892 be considered in their entirety.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Vartanian whose telephone number is 703.305.8698. The examiner can normally be reached on 9-5:30 Mondays to Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703.305.4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harry Vartanian
Examiner
Art Unit 2634

HV

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600